PCB LOGIC CLOCK DESIGN
FOR LOW DPPM (DEFECTIVE PARTS PER MILLION)

APPLICATION NOTES

ASIC manufacturers use an internal oscillator cell. Proper selection of five external capacitors, resistors, and crystal load can increase frequency stability, reduce cost, and reduce dppm.

Two Barkhausen rules are also necessary for oscillation:

- The summation of the phase shifts around a closed loop must be N*360 degrees where N is an integer (0, 1, 2, ...)
- Summation of the gains around a closed loop must be equal to or greater than 1.

Crystal Equivalent Circuit. Fig 1 is the equivalent circuit for a crystal plus external load.

Oscillator Schematic. Most ASIC use the Pierce oscillator configuration. Ref Fig 2.

Pi Capacitors: Pi cap reactance values should be in the low hundreds of ohms and should be approximately equal to the output impedance of the ASIC cell. Oscillator cells designed for lower frequency AT-cut crystals have ~300 to 500 ohms Thevenin output resistance (Rout). Higher frequency fundamentals are ~100 to 300 ohms.

Pi caps are changed as a function of crystal load and VDD. Pi caps are usually the same value or C1 may be slightly smaller than C2. Ref Table I.

Rd selection Rd, sometimes called a phase shift resistor, is between IC output and crystal. The phase shift resistor has 4 functions:

- Reduce crystal power
- Reduce C2 output loading
- Shift phase
- Increase frequency stability

If Rd equals Xc2, a Bode plot would show there is fast rate-of-change of phase at the 360 deg oscillation requirement. Fast rate-of-change of phase is critical for good frequency stability. Ref Fig 3.

Rout and Rd are in series. The series combination is in parallel with C2. Select Rd = Rout = Xc2 unless cell has insufficient drive capability. First select C2, then select Rd.

Rout in series with Rd are shunting C2 (Rout + Rd) // Xc2). With Rd=Rout=Xc2, we have a loaded Q of only 2. Design for Q of 2, but you may accept a Q of 1.

Rf Selection. Most ASIC has internal Rf resistor. If not, choose Rf between 100k and 500k ohms.

Crystal Load. With good oscillator PCB layout and VDD = +5 VDC, Cstray is ~6 to 7 pf. With VDD = +3.3 VDC or lower, Cstray is ~3 pf.

$$Cload = \frac{C1 * C2}{C1 + C2} + Cstray$$

Crystal Load vs Frequency. Crystal load is a function of frequency. Suggested values are in Table II.

C1, C2 Selection. Table III has C1 and C2 calculations for specified loads. Stray capacitance has many variables; however Table III will get most crystals close to frequency.

Circuit Waveshape Verification. Check circuit waveshapes with a non-loading FET probe (or equiv). With Rd=Rout=XC2, top of C2 should be a poorman's sinewave. Peak to peak amplitude should be ~70% of VDD.

If Rd is omitted (sometimes done at higher frequencies or with low output drive), layout should still include Rd as a short. If Rd is a short, top of C2 should be a squarewave with rounded corners. Sharp rise and fall times are indications of excessively high drive or insufficient C2.

If C2 is too small, a low resistance crystal may have high ESR.

$$ESR = Rm * \left(1 + \frac{Co}{Cload}\right)^2$$

Less than full amplitude squarewave is an indication that Rd may be too large or C2 may be too large and is passing signal to ground.

Starting Voltage Checks. Continuously monitor the waveshape at the IC output for any abnormalities during all starting tests. This may be difficult on a PCB unless PCB regulated supply is overridden.

Low voltage starting checks should be made by slowly increasing VDD from 0 volts. Perform this test first to detect and prevent effects of a sleepy crystal. Expect that oscillator should be started at half the nominal VDD. If not, loading on the IC may be too large or the IC may have insufficient gain. Continue this test up to nominal VDD plus 1.5 VDC.

High voltage starting checks are made by applying numerous VDD step functions starting with VDD plus 1.5VDC and slowly decrease to low voltage starting point. Intermittent starting problems may be an indication that Co or Cstray are too large.

Medium voltage starting checks are made by switching the power supply switch on and off. Perform this test from half VDD to VDD plus 1.5 volts.

Negative Resistance Testing. Negative resistance is similar to circuit gain. Test the circuit by installing a resistive pot in series with an AVERAGE crystal. Do not perform this test on a known bad crystal. Negative resistance is the value of the pot plus the crystal's series resistance.

$$-r = Rpot + Rs$$

Crystal Power. While the crystal is disconnected, attach a current probe and measure crystal current. Do not exceed maximum rated power of crystal unit.

$$\text{Crystal Power} = Irms^2 * Rm$$

Adjusting –r. Where gm is the transconductance of the inverter and:

$$-r = gm * \left(\frac{1}{\omega C1} + \frac{1}{\omega C2}\right) \qquad \omega = 2\pi * \text{frequency}$$

By making C1 and C2 smaller, we can raise the negative resistance. Caps too small will cause high ESR and reduced phase shifting.

Circuit Margin. Circuit margin is defined as the absolute value of negative resistance |-r| divided by the average value of ESR.

$$CM = \frac{|-r|}{ESR_{avg}}$$

For low dppm, circuit margins should be at least 10. Some approximate values taken from experimental data can be found in Table III.

Temperature Testing. Quick temperature testing can be performed using a few seconds of freeze mist (or a can of duster spray held upside down) and a hair dryer. Test only when circuit is returning to room ambient.

Summary. Oscillator designers and crystal suppliers working together can assemble circuits having single digit dppm failure rates. This starts with the oscillator being designed on sound basics and working with a crystal supplier, who designs, manufactures and controls his production. On first designs, it is suggested that the schematic or even the PCB should be sent to the crystal supplier for circuit board matching.

CRYSTAL LOAD	+3.3 VDC		+5 VDC	
	C1	C2	C1	C2
6	5	6		
7	8	8		
8	10	10	5	5
10	12	15	6	8
11	15	18	8	10
12	18	22	10	12
14	22	22	15	15
16	22	27	18	22
18	27	33	22	27
20	33	39	27	27
22	39	39	33	33
30	56	56	47	47
32	56	68	47	56

Table 1: C1 & C2 selection for Crystal Load

LOAD	FREQUENCY RANGE
20 PF	---> 5 MHZ
18 PF	5 TO 10 MHZ
16 PF	10 TO 15 MHZ
14 PF	15 TO 20 MHZ
12 PF	20 to 30 MHz
10 PF	30 to 40 MHZ
8 PF	40+ MHZ

Table 2: Suggested Loads for Fundamental Crystals

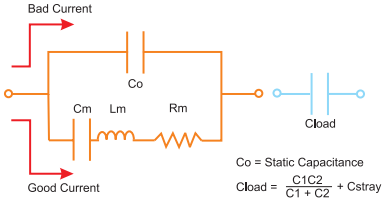

Figure 1: Equivalent Circuit of a Crystal

CKT MARGIN	EXPECTED DPPM
1.5	Runs poor w/ best xtals
2	Serious operating pblms
3	Intermittent starting
5	~1,000 dppm
10	~100 dppm
15	~25 dppm
20	~15 dppm
25	Single digit dppm

Table 3: Expected DPPM

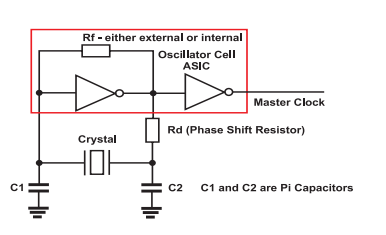

Figure 2: Oscillators Schematic

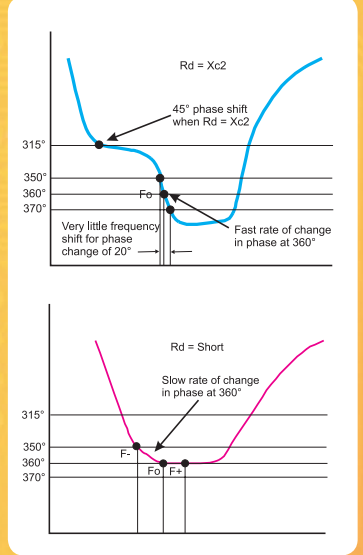

Figure 3: Bode Plots with and without Rd