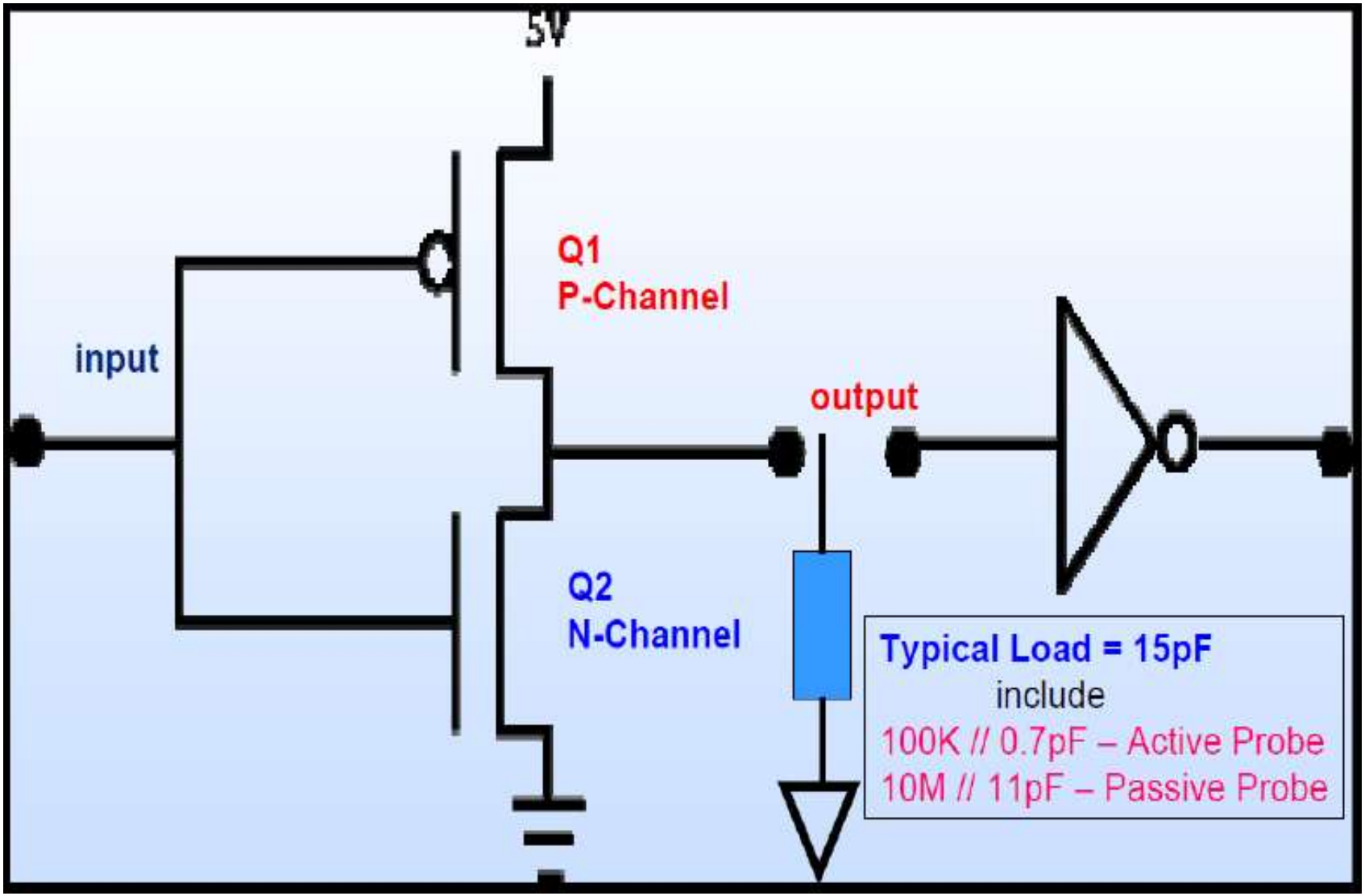
AKER
Accurate Kinetic Energy

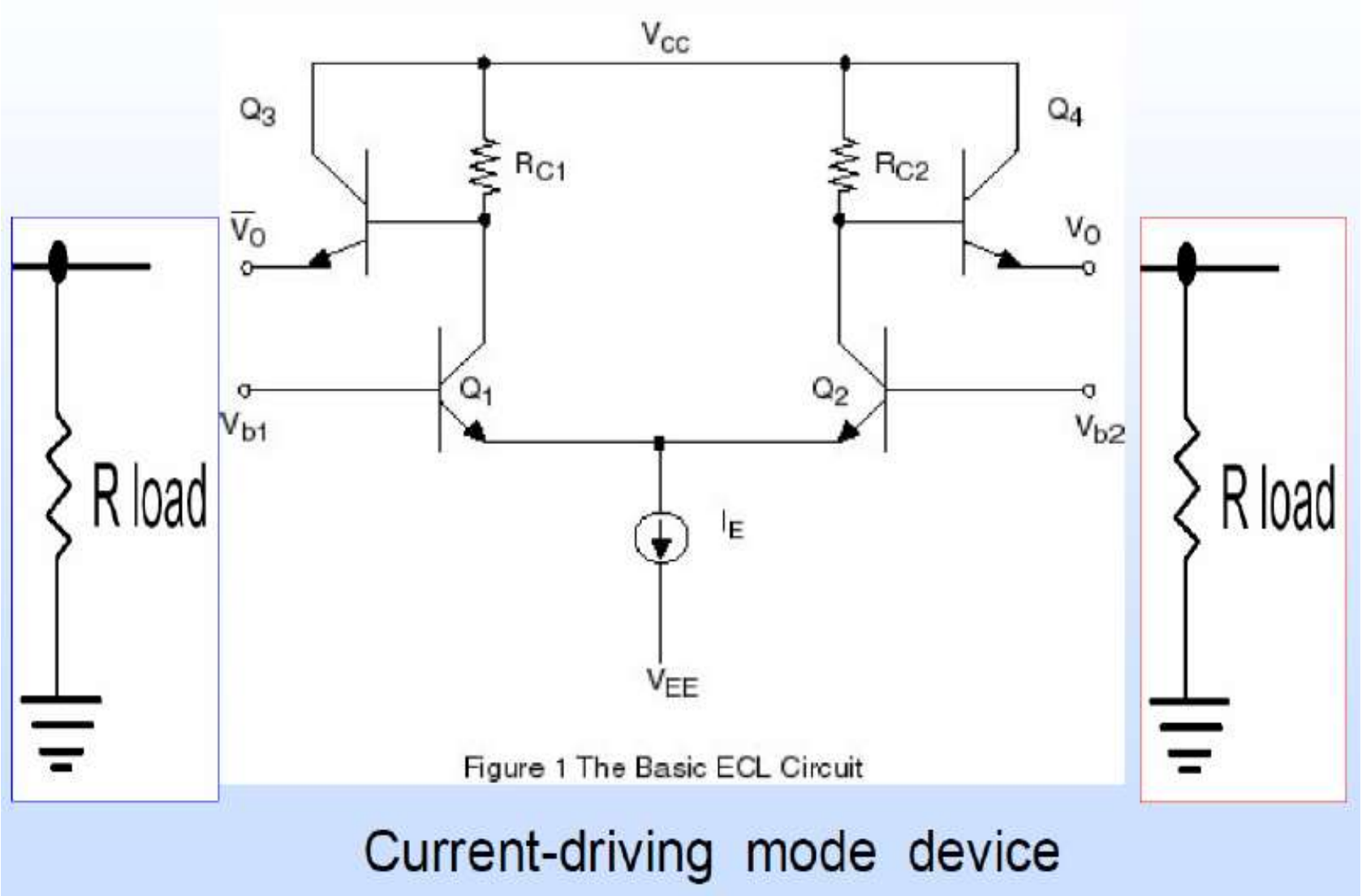
What is the LVDS?

What is the LVPECL?

CMOS output LOGIC



LVPECL/LVDS output circuit



Balanced Device vs Unbalanced Device

- TTL / CMOS OSC → Unbalanced Device
  operating in "saturation region" in TTL logic
- LVPECL / LVDS OSC → Balanced Device
  operating in "active region" in ECL logic
  → switching fast & suitable for "high frequency applications"

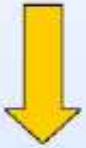
Advantage for Balanced Device

- High noise immunity
- Low power consumption
- Low radiated noise
- High integration density

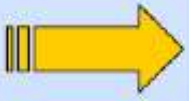
LVPECL/LVDS Signal Analysis

LVPECL & LVDS signal : DC-signal + AC-signal

- Vc = (½) * (V1 + V2) --- Common Mode Signal
- Vd = V1 – V2 --- Differential Mode Signal

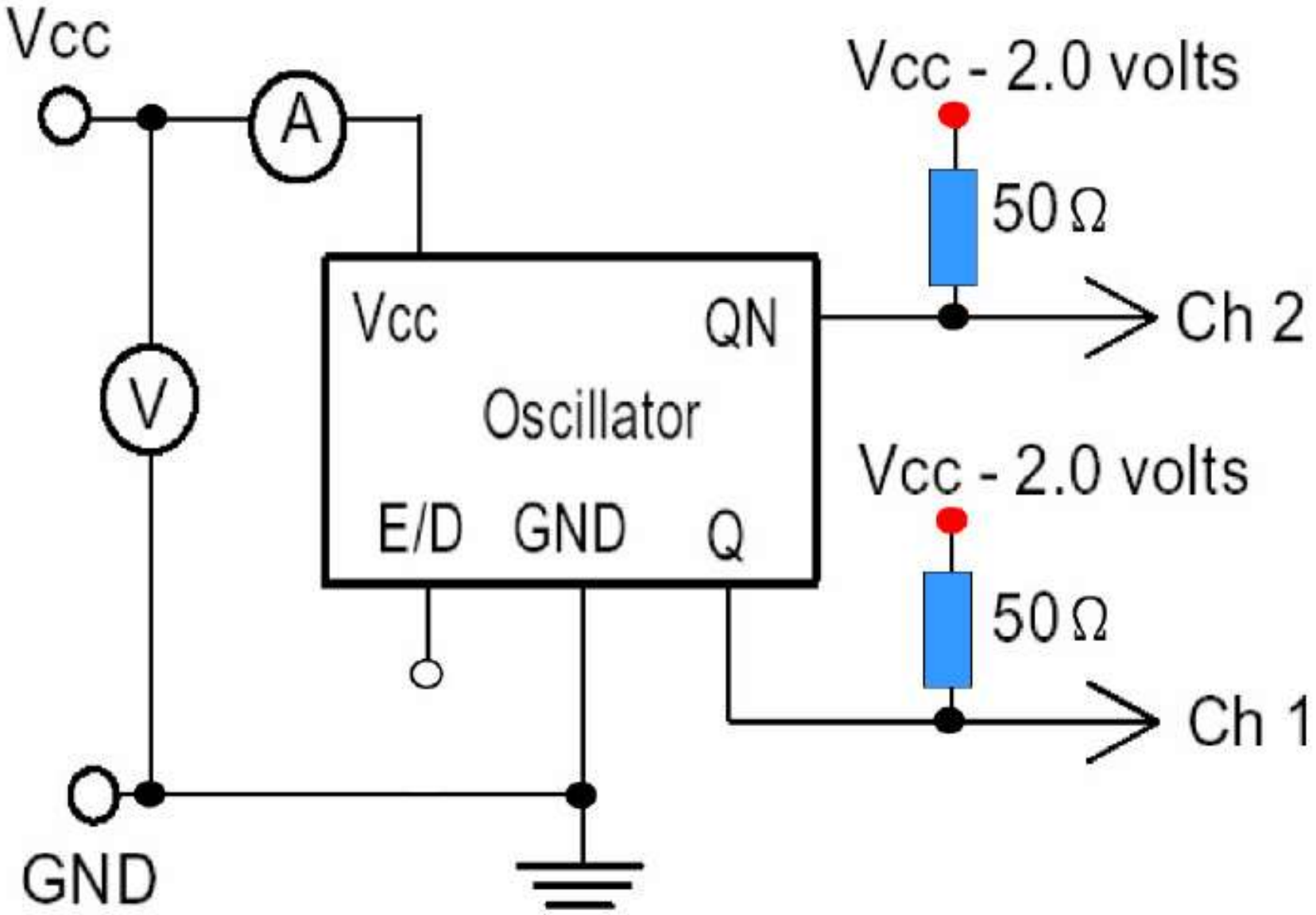


- V1 = Vc + Vd/2
- V2 = Vc - Vd/2

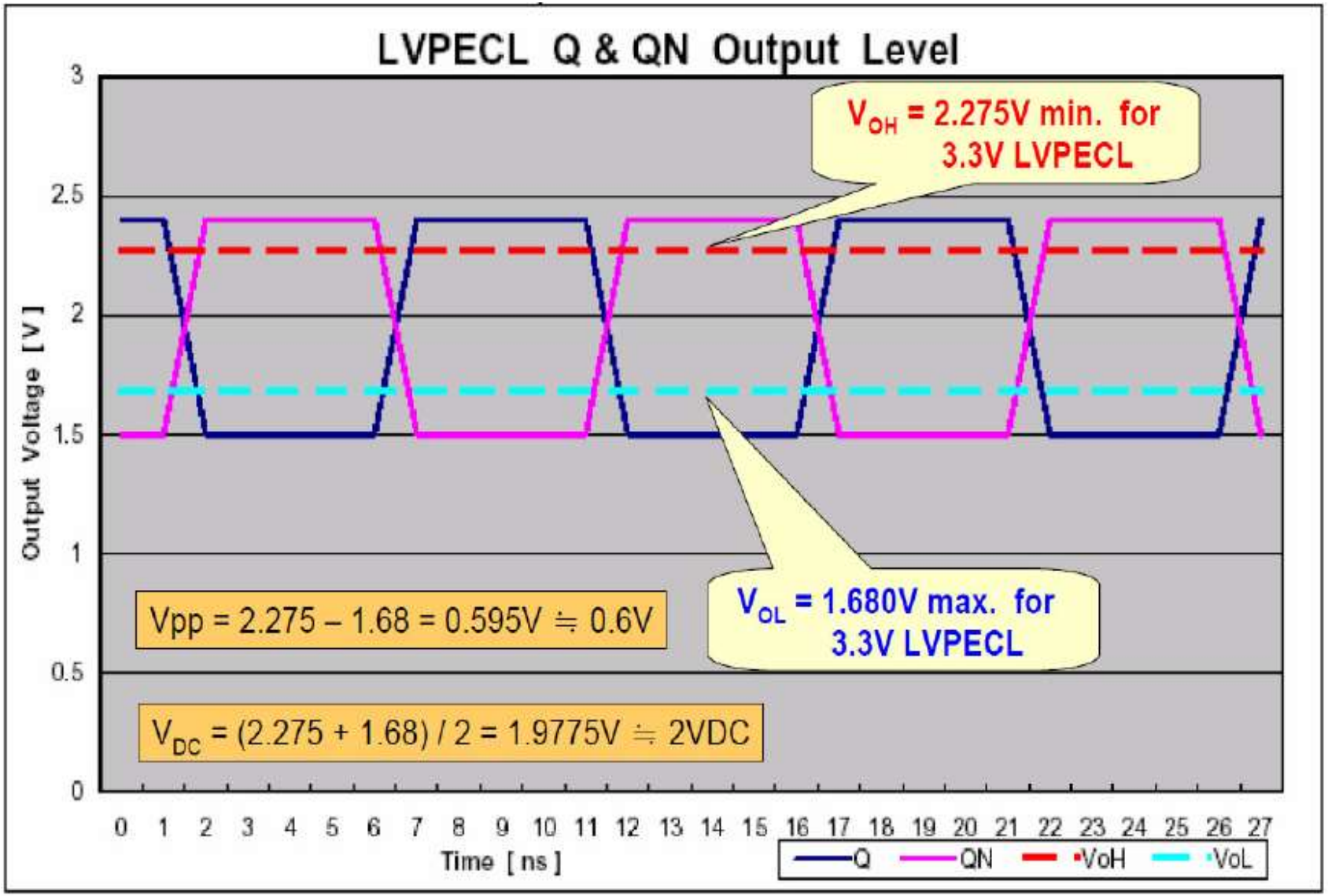


Signal analysis can be implemented easily by math. tool

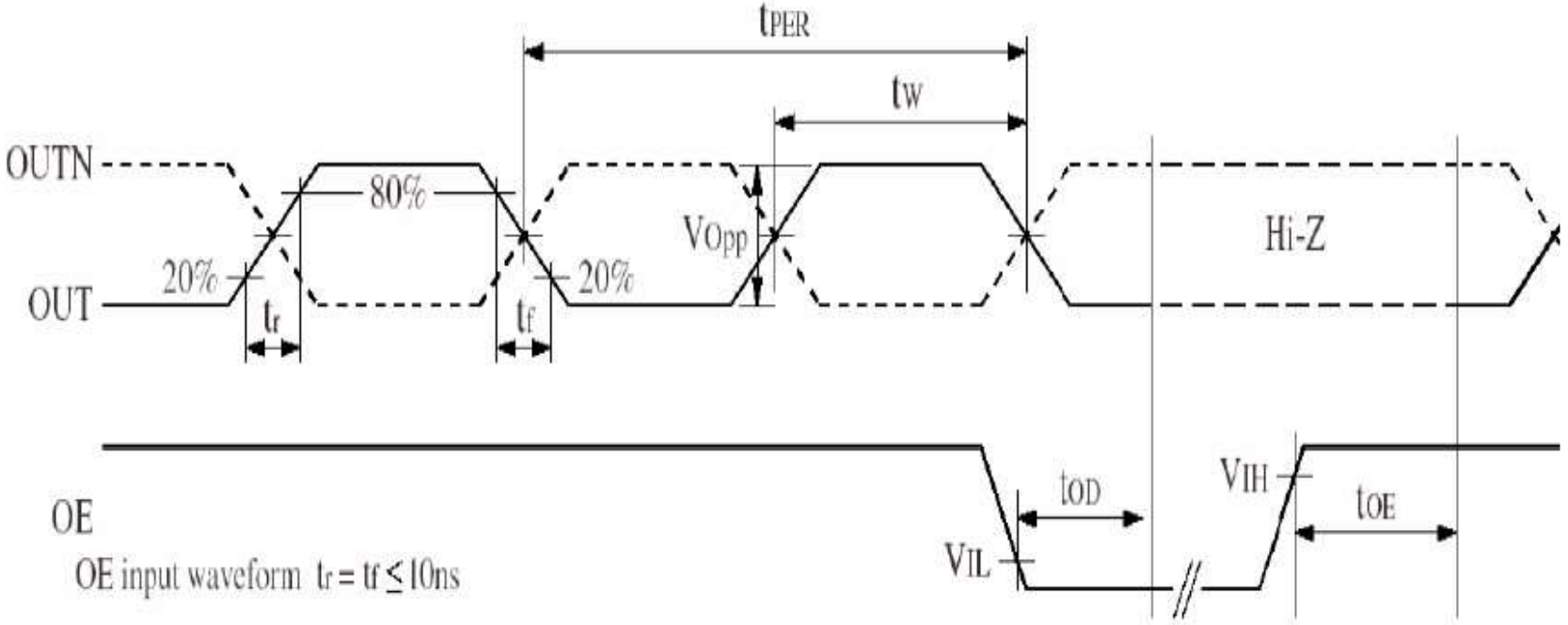
LVPECL Testing circuit



LVPECL Output Level & Waveform



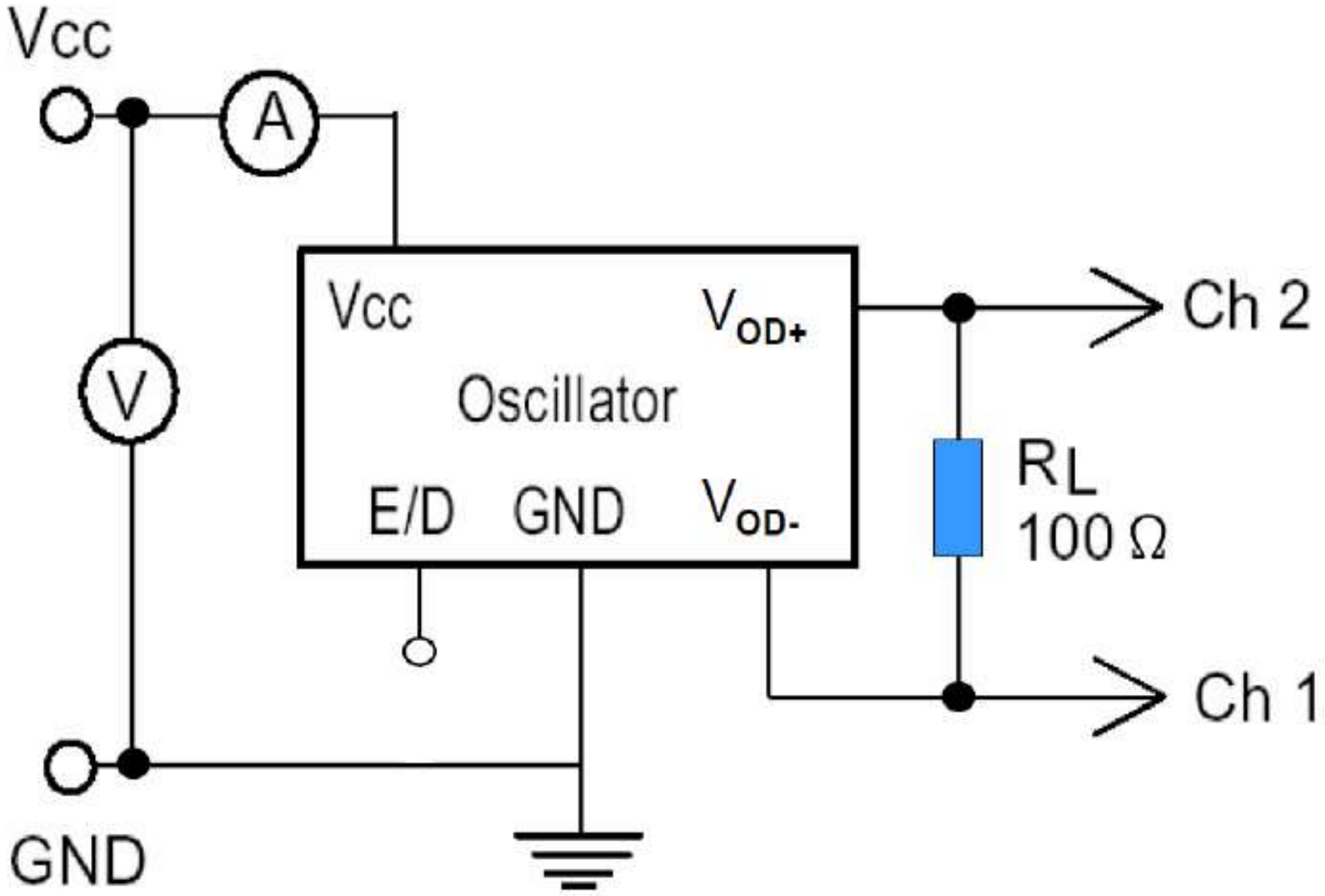
LVPECL Output Waveform



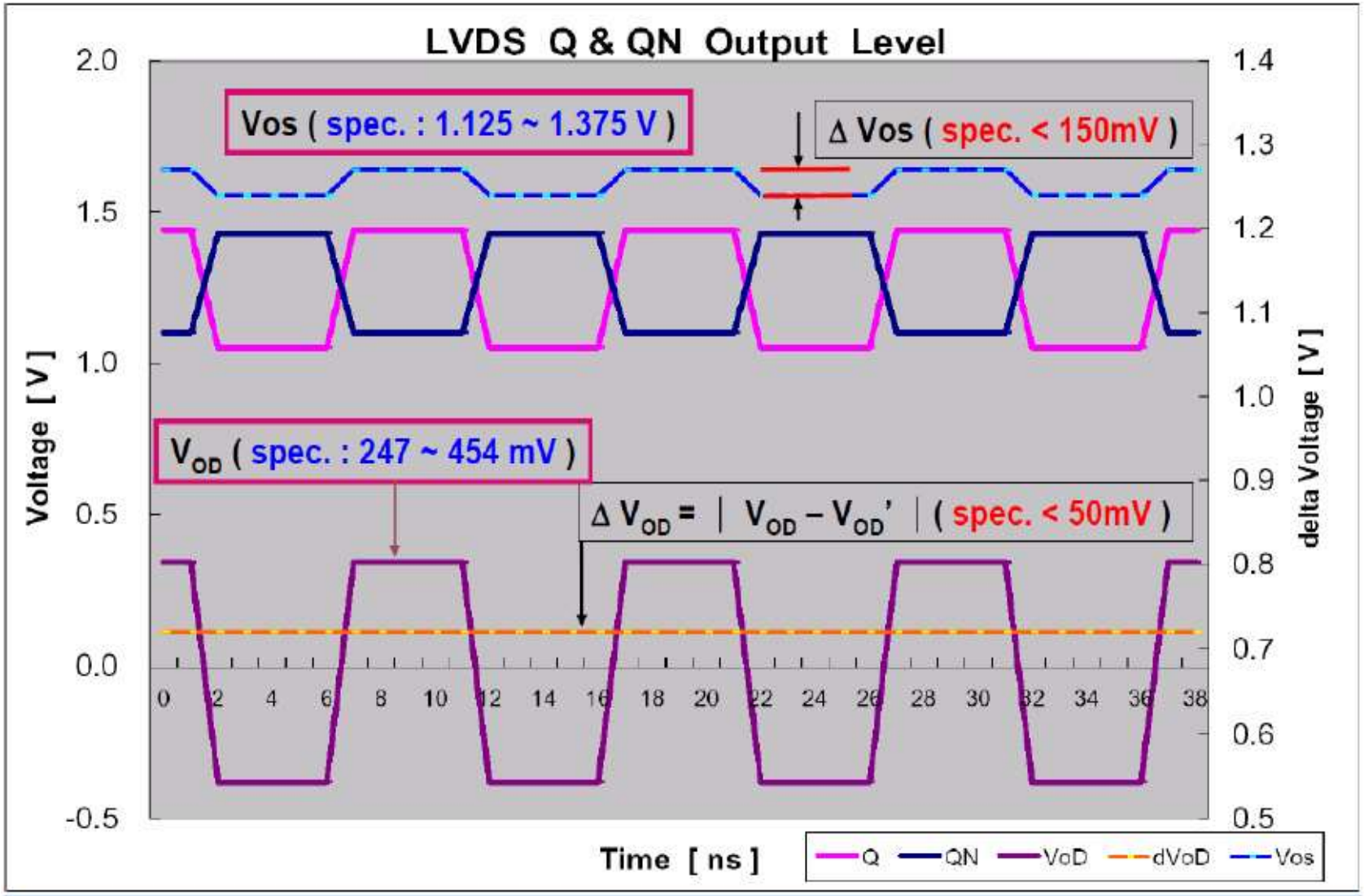
DUTY1 = $100t_W/t_{PER}$ (%) @ crossing point
DUTY2 = $100t_W/t_{PER}$ (%) @ 50% waveform

Timing chart

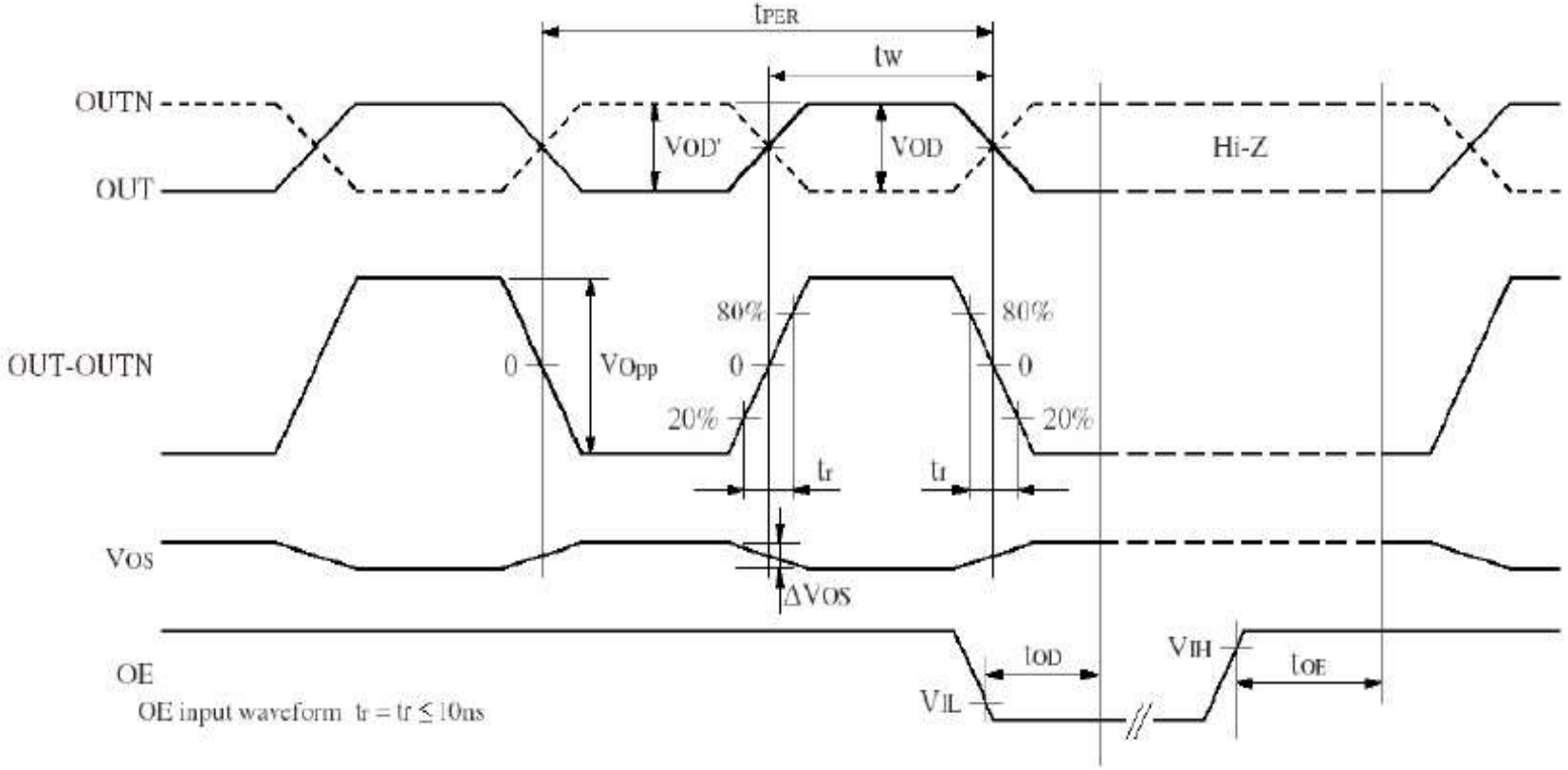
LVDS Testing circuit



LVDS Output Level & Waveform



LVDS Output Waveform

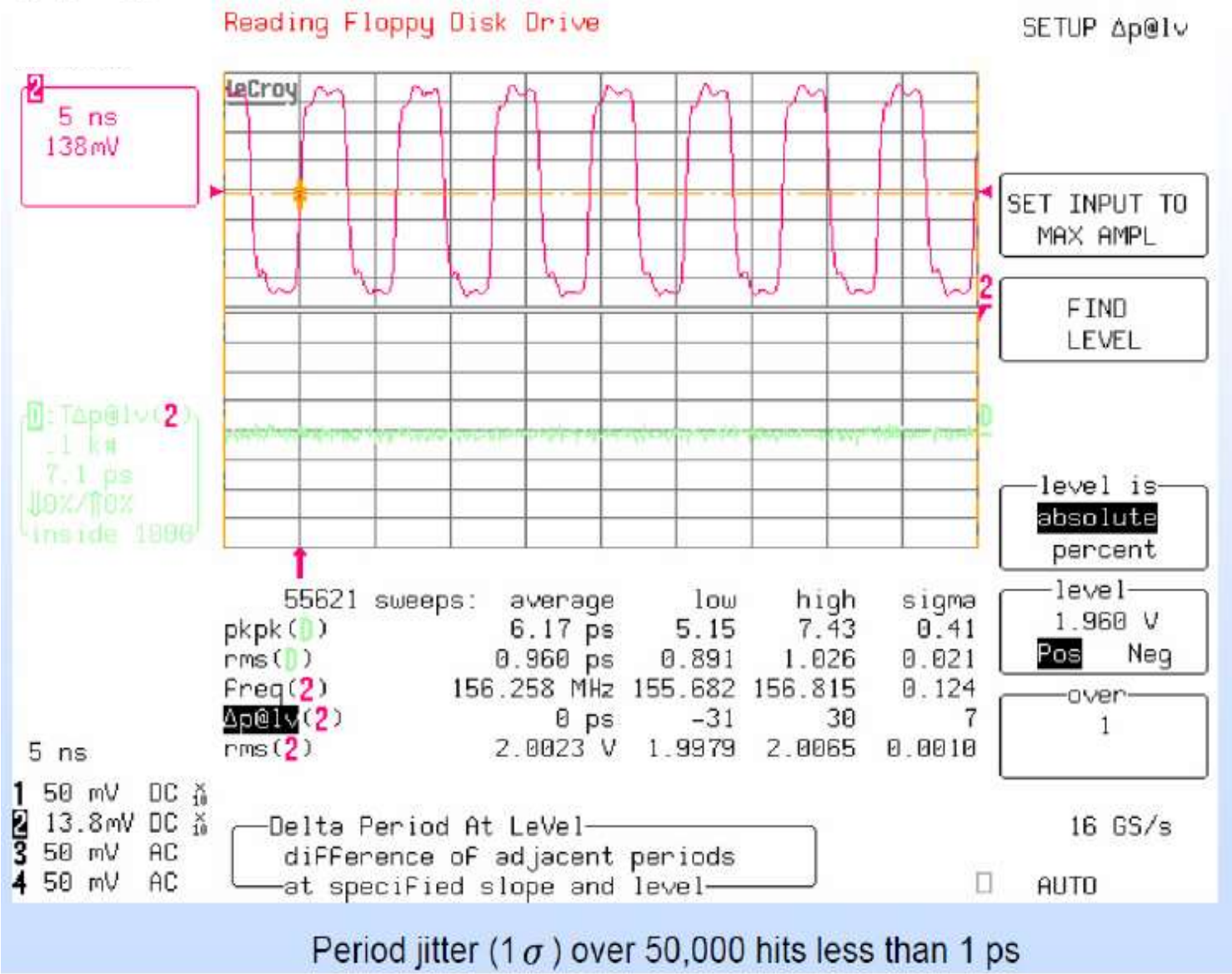


$DUTY = 100t_W/t_{PER}$ (%) @ crossing point

$\Delta V_{OD} = |V_{OD}' - V_{OD}|$

Timing chart

Typical period jitter test data



Period jitter (1 σ) over 50,000 hits less than 1 ps